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DECODER ARCHITECTURES FOR LOW-DENSITY PARITY-CHECK CODES



VDM Verlag Aug 2011, 2011. Taschenbuch. Book Condition: Neu. 220x150x7 mm. This item is printed on demand - Print on Demand Neuware - Recently, LDPC codes are considered for applications such as high-speed satellite and optical communications, the hard disk drives, and high- density flash memory based storage systems, which require that the codes are free of error-floor down to extremely low bit error rates. FPGAs are usually used to evaluate the error performance of codes. However, existing FPGA-based LDPC...

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- Authored by Xiaoheng Chen
- Released at 2011



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Simply no phrases to clarify. It is really basic but surprises from the 50 percent of the ebook. Once you begin to read the book, it is extremely difficult to leave it before concluding.

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